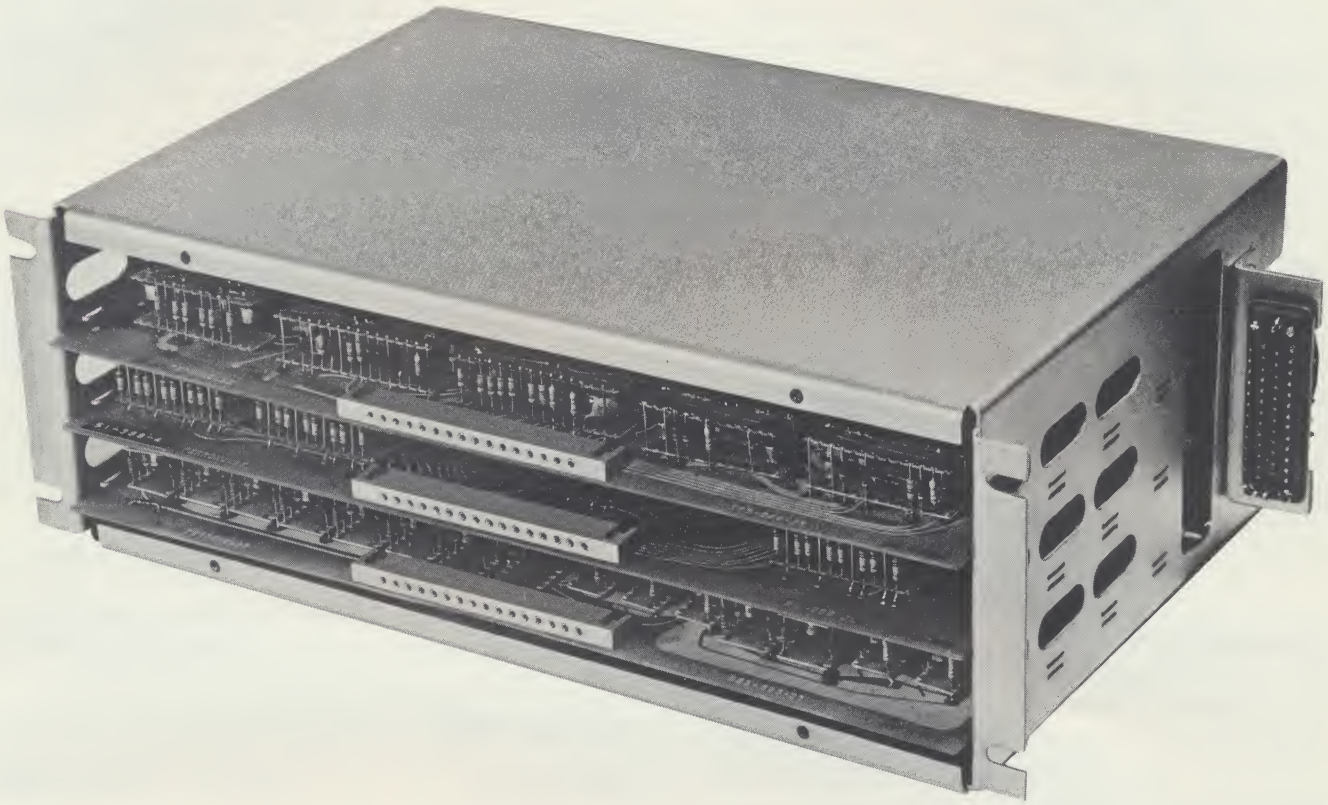
FERROXCUBE
CORPORATION OF AMERICA
ENGLEWOOD, COLORADO

MEMORY SYSTEMS
TYPE FX-12/C
Bulletin 1808



FEATURES:

- Size – up to 512 Words x 8 bits
- Cycle Time – 4 microseconds full cycle
- Access Time – $<$1.5 microsecond
- All silicon cordwood module motherboard construction
- LTC Cores for wide operating temperature range 0-65°C
- Wide voltage margins ± 10%
- Low cost
- MTBF – 7100 hours per Mil Std 217

DESCRIPTION

Ferroxcube's FX-12/C Memory System is a small, 512 words x 8 bit, coincident current memory including stack, sense preamp, x, y and inhibit drivers, data register and timing control circuitry. It is specifically designed for applications such as code conversion, speed buffering, or general purpose random access memory where low cost and extreme reliability are the primary design considerations. The unique design using standard cordwood circuit modules produced in large volume makes possible costs which are competitive with core rope, delay line, flip-flop, relay, or other small capacity but less versatile memory techniques. The circuit modules are mounted on three plug-in printed circuit cards, one each for Timing and Data Control, Core Memory and Sense Preamps and Address Selection and Drive.

SYSTEM SPECIFICATIONS

CYCLE TIME – 4 μsec full cycle,

ACCESS TIME – ≤ 1.5 μsec-typically 1 μsec

CAPACITY/CONFIGURATION

Word Size	Bit Size	Memory System Model No. with 200Ω collector R.	Memory System Model No. with 750Ω collector R.
512	8	52 – 137	52 – 146
256	8	52 – 141	52 – 147
128	8	52 – 142	52 – 148

INPUT SIGNALS

Logic "O"	≤ + 1.5 Volts at 3 ma
Logic "1"	≥ + 3.0 Volts at .5 ma
Data Input	8 lines, single rail. Must be available from 200 nsec. before start of any cycle and remain for 1.5 μs.
CLEAR/WRITE	Positive-going pulse, to begin Clear/Write cycle, $T_r \leq 150$ nsec. Positive-going edge starts cycle. Pulse must remain for 1.5 to 2.0 μs.
READ/RESTORE	Positive-going pulse, to begin Read/Restore cycle. $T_r \leq 150$ nsec. Positive-going edge starts cycle. Pulse must remain for 1.5 to 2.0 μs.
Address Input	9 Lines, single rail. Must be available from 200 nsec. before start of any cycle and remain for more than 3.5 μs.

OUTPUT SIGNALS

Logic "O"	0.5 Volts (± 0.5 V) at 10ma maximum from a saturated transistor.
Logic "1"	+ 4.5 Volts (± 10%) through 200 ohms to + 4.5 *
Data Output	8 Lines, single rail. Will be available not later than 1 μs after the Read/Restore Command.

* Logic "1" output level is nominally specified at + 4.5 Volts to show compatibility with integrated circuits; however, this can be varied to suit the application by specifying the resistor in the collector of each output stage as called out in the following table.

OUTPUT LOGIC "1" LEVEL	COLLECTOR RESISTOR
+ 3.5 Volts to + 4.5V	200 ohms
+ 5.0 Volts to + 12.0V	750 ohms

MODES OF OPERATION

READ/RESTORE – The information stored in a given address location is read and restored in this location.

CLEAR/WRITE – The information stored in an address location is erased by a read operation (preventing the information from the cores entering the input/output register), and new information is written in this location.

POWER REQUIREMENTS

VOLTAGE	STATIC STABILITY INCLUDING RIPPLE	DYNAMIC STABILITY	MAXIMUM DUTY CYCLE CURRENT
** +4.5V	±2%	±2%	.2A
−12V	±2%	±2%	.2A
+12V	±2%	±2%	2.4A

** Logic Level voltage shown is for integrated circuits. Any voltage from + 3.5V to + 12V may be used.

MEMORY TESTS

Test Patterns:

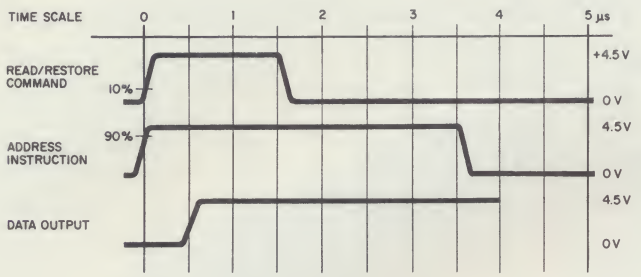
All zeros
All ones
Double Checkerboard
Double checkerboard complement
Random

Test Patterns are circulated in memory at 0°C, 25°C and 65°C. During test each voltage is varied ± 10% of its nominal value with all possible combinations.

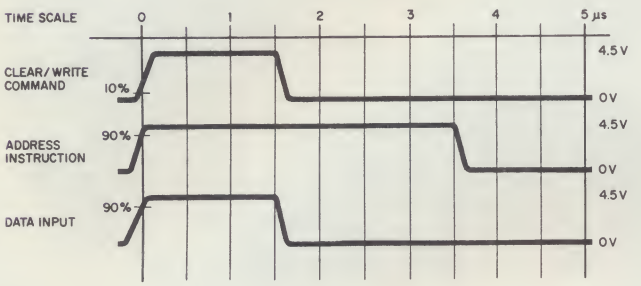
ENVIRONMENTAL CHARACTERISTICS

Operating temperature range – 0°C to 65°C
Humidity – 90%

TIMING DIAGRAMS



READ/RESTORE CYCLE

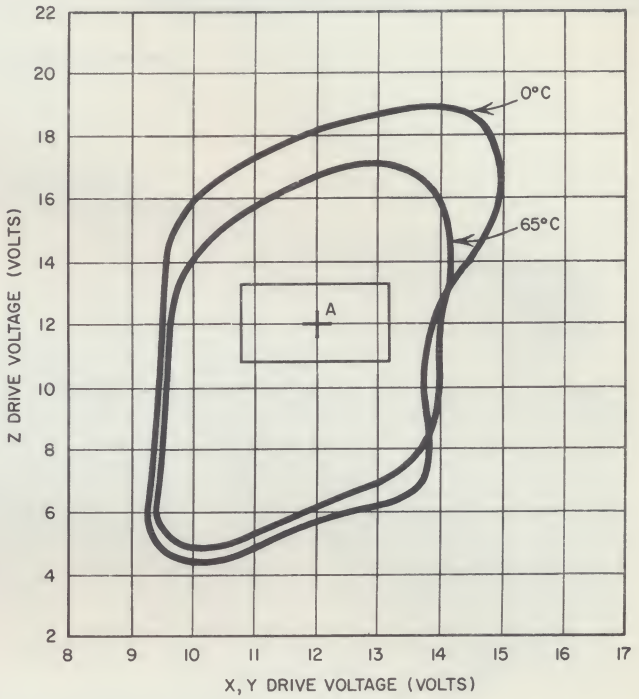


CLEAR/WRITE CYCLE

MECHANICAL FEATURES

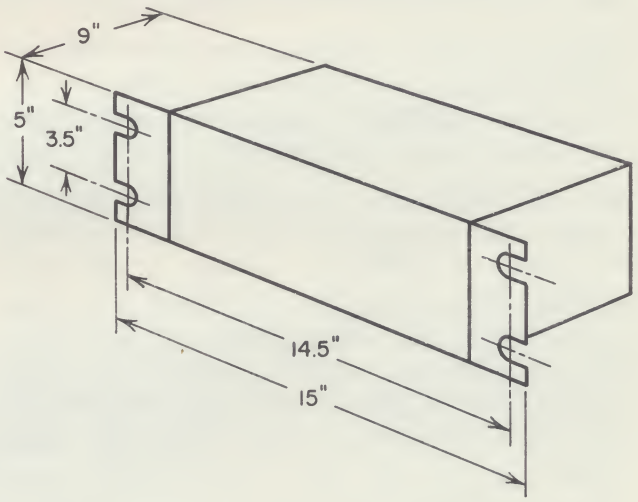
Cordwood module construction
Wire Wrap Back Panel
Glass epoxy printed circuit boards
Gold Iridite Finish
Rugged Construction
41 easily accessible test points
Weight: Less than 7 pounds

SCHMOO PLOT ANALYSIS

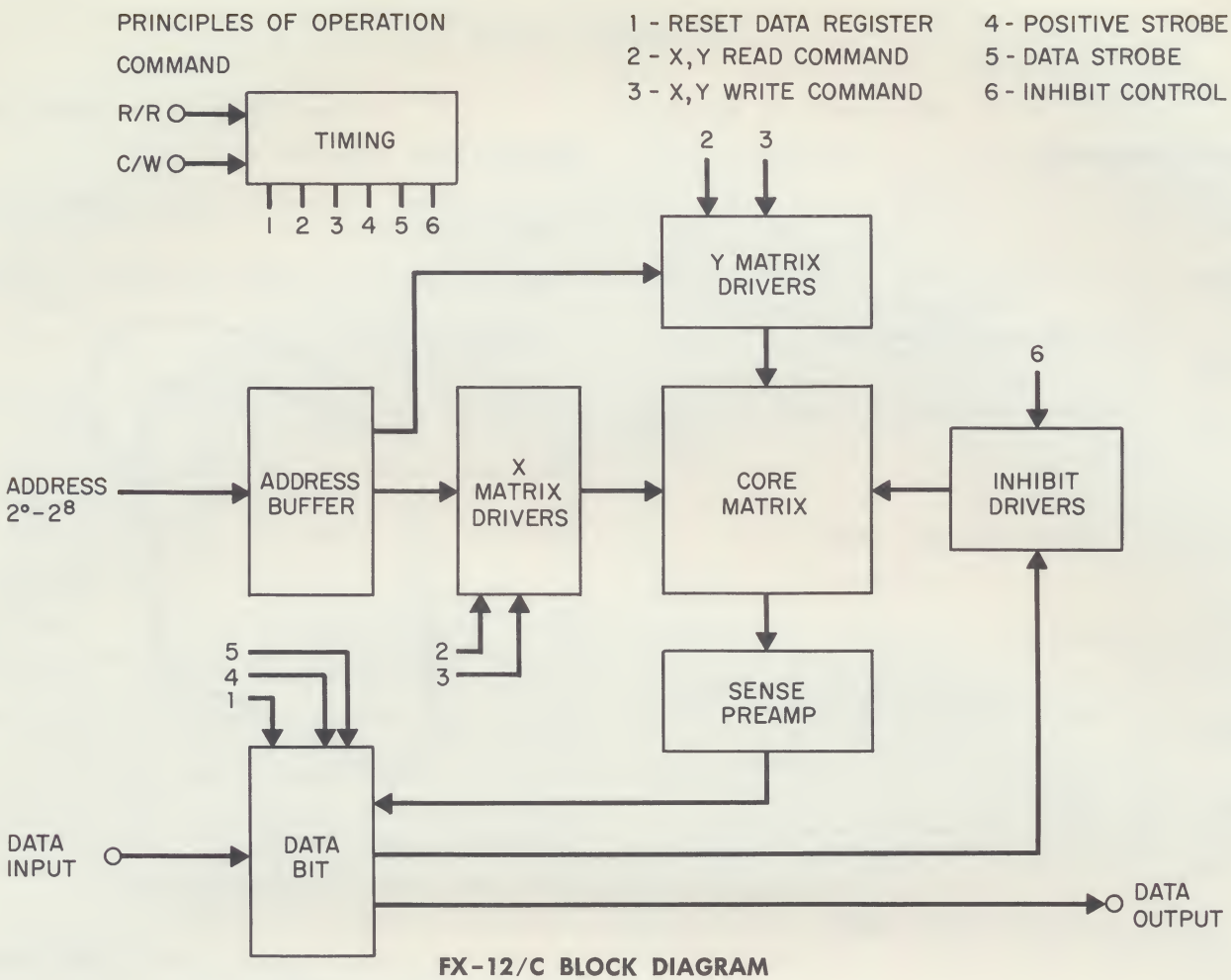


Shown is an actual "Schmoo" plot for the FX-12/C Memory System in which the locus of x, y drive current vs inhibit drive current for a particular value of noise threshold, strobe time and operating temperature is plotted. Point A (+ 12 Volts) indicates the nominal operating point of the FX-12/C. The rectangle represents ± 10% variations in drive voltage.

MOUNTING DIAGRAM



AN ADAPTER PANEL FOR 19" RACK MOUNTING IS AVAILABLE. HEIGHT 5¼" WITH STANDARD EIA MOUNTING HOLES.



FX-12/C BLOCK DIAGRAM

PRINCIPLES OF OPERATION

Upon the receipt of a Read/Restore or Clear/Write Command, the timing circuitry generates six internal commands. Command number 1 resets the data register, thus clearing information which had been entered into the Data Register as a result of a previous cycle.

Command number 2 is defined as the X, Y Read Command which along with the decoded Address Instruction, generates a "Read" current to switch the proper group of cores in the Core Matrix.

When the ferrite cores are switched they generate a voltage which is applied to the Sense Preamplifiers. The Sense Preamplifier is basically a differential amplifier which brings the 50 millivolt core signal to an internal logic level. During the X, Y Read Command a pulse is generated to strobe (gate) either the data from the Core Matrix or the data from the Data Input lines into the Data Bit Module, (Data Register).

Timing Command 4 gates data from the Core Matrix during a Read Restore operation and Command 5 gates data from the Data Input lines during a Clear Write operation.

After data from either the Core Matrix or the Data Input lines has settled in the Data Register, Command 3 and 6 are generated coincidently. Command 3 along with the decoded Address Instruction, generates a current via the Matrix Drivers of sufficient magnitude to switch the proper group of cores back to the Logic "1" state. To store information other than a Logic "1" in the Core Matrix, Command 6 in association with the data present in the Data Register generates a current via the Inhibit Drivers sufficient in magnitude to oppose the switching of the selected group of cores. That is to say, when a Zero is to be stored in a particular memory location, the associated Inhibit Driver is turned on.

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